WHAT IS CLAIMED IS

1. A cache system inside the peripheral device interface control chip of a computer system that includes a memory unit, a central processing unit (CPU), a CPU bus, a peripheral device bus and at least one peripheral device, comprising:

a data buffer located within the control chip for holding a data stream read from the memory unit so that data required by the peripheral device bus are provided, and when the data stream is synchronous with data in a corresponding address within the memory unit, the data stream is retained, and when any one of the peripheral devices demands data already in the data stream, data within the data stream can be immediately provided by the data buffer so a latency period for retrieving the data stream from memory again is reduced; and

a peripheral device interface controller installed within the control chip for determining if the data stream includes data demanded by a particular peripheral device and determining if the data stream is synchronous with data in the corresponding address, then retrieving the data stream from the memory unit and putting the data in a data buffer, and finally switching a state of that portion of the data buffer having data stream therein.

2. The cache system of claim 1, wherein the peripheral device interface controller further includes transmitting a probe-hit-read signal to the central processing unit.

3. The cache system of claim 1, wherein the peripheral device interface controller further includes receiving signals emitted when data are written from the peripheral device bus to the corresponding address.

4. The cache system of claim 1, wherein the peripheral device interface controller further includes receiving signals emitted when data are written from the CPU bus to the corresponding address.

5. The cache system of claim 1, wherein the peripheral device interface controller further includes receiving signals emitted when data are read from the corresponding address to the CPU bus.

6. The cache system of claim 1, wherein the data buffer comprises at least one line.

7. The cache system of claim 6, wherein the data buffer has altogether eight lines.

8. The cache system of claim 7, wherein the eight lines are divided into four transmission blocks each having two lines.

9. The cache system of claim 6, wherein each line comprises of 32 bytes.

10. A method of synchronization data transmission between cache memory inside a peripheral device interface control chip and external device that can be applied to a computer system having a memory unit, at least one central processing unit, a control chip, a peripheral device bus, a CPU bus and at least one peripheral device, wherein the control chip includes a peripheral device interface controller and a data buffer and the central processing unit uses a MOESI protocol, a memory data stream becomes a cache data stream when the memory data stream within the memory is read into the central processing unit, and the memory data stream becomes a buffer data stream when the memory data stream is read into the data buffer, further comprising the steps wherein:

when the cache data stream is in a modified state and if the data buffer executes a read operation from an address in memory that corresponds to the cache data stream, the peripheral device interface controller inform the central processing unit to set the cache data stream into an owner state; and

when the cache data stream is in an exclusive state and if the data buffer executes a read operation from the corresponding address, the peripheral device interface controller will inform the central processing unit to set the cache data stream into a shared state.

11. The data synchronization method of claim 10, further comprising the steps wherein:

the data buffer is set to an empty state on initialization;

when the peripheral device interface controller reads the buffer data stream into the data buffer according to the requirement of the particular peripheral device, a buffered data portion of the data buffer that includes the buffer data stream is set to a clean-unaccessed state;

when the buffered data portion is in a clean-unaccessed state and if the peripheral device interface controller detects from the CPU bus a write or a read operation using the corresponding address, the buffered data portion is set to a dirty-unaccessed state;

when the buffered data portion is in the clean-unaccessed state, if the peripheral device interface controller detects from the peripheral device bus a write operation using the corresponding address, the buffered data portion is set to a dirty-unaccessed state;

when the buffered data portion is in the clean-unaccessed state and if the particular peripheral device that demands the buffer data stream reads the buffer data

stream from the buffered data portion, the buffered data portion is set to a clean-accessed state;

when the buffered data portion is in a dirty-unaccessed state and if the particular peripheral device that demands the buffer data stream reads the buffer data stream from the buffered data portion, the buffered data portion is set to an empty state;

when the buffered data portion is in a clean-accessed state and if the peripheral device interface controller detects from the CPU bus a read or a write operation using the corresponding address, the buffered data portion is set to an empty state; and

when the buffered data portion is in the clean-accessed state and if the peripheral device interface controller detects from the peripheral device bus a write operation using the corresponding address, the buffered data portion is set to an empty state.

12. The data synchronization method of claim 10, wherein a probe-hit-read signal is transmitted from the peripheral device interface controller to the central processing unit when a buffer data stream is read from the peripheral device interface controller to the data buffer.

13. The data synchronization method of claim 12, wherein the probe-hit-read signal further includes the corresponding addresses.

14. A method of synchronization data transmission between cache memory inside a peripheral device interface chip and external device that can be applied to a computer system having a memory unit, at least one central processing unit, a control chip, a peripheral device bus, a CPU bus and at least one peripheral device, wherein the control chip includes a peripheral device interface controller and a data buffer, and a data stream becomes a buffer data stream when the memory data stream inside the memory is read into the buffer data, comprising the steps of:

setting the data buffer to an empty state on initialization;

settting the buffered data portion of the data buffer that includes the buffer data stream to a clean-unaccessed state when the peripheral device interface controller reads the buffer data stream into the data buffer according to the requirement of the particular peripheral device;

setting the buffered data portion to a dirty-unaccessed state if the peripheral device interface controller detects from the CPU bus a write or a read operation using the corresponding address when the buffered data portion is in a clean-unaccessed state;

setting the buffered data portion to a dirty-unaccessed state if the peripheral device interface controller detects from the peripheral device bus a write operation using the corresponding address when the buffered data portion is in the clean-unaccessed state;

setting the buffered data portion to a clean-accessed state if the particular peripheral device that demands the buffer data stream, reads the buffer data stream from the buffered data portion when the buffered data portion is in the clean-unaccessed state;

setting the buffered data portion to an empty state if the particular peripheral device that demands the buffer data stream, reads the buffer data stream from the buffered data portion when the buffered data portion is in a dirty-unaccessed state;

setting the buffered data portion to an empty state if the peripheral device interface controller detects from the CPU bus a read or a write operation using the corresponding address when the buffered data portion is in a clean-accessed state; and

setting the buffered data portion to an empty state if the peripheral device interface controller detects from the peripheral device bus a write operation using the corresponding address when the buffered data portion is in the clean-accessed state.

15. The data synchronization method of claim 14, wherein a probe-hit-read signal is transmitted from the peripheral device interface controller to the central processing unit when a buffer data stream is read from the peripheral device interface controller to the data buffer.

16. The data synchronization method of claim 15, wherein the probe-hit-read signal further includes the corresponding addresses.